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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Khan, Asif Pagan, Annette Pekkala, Richard Pettey, Christopher Utley, Robert	Examiner:	unknown
Docket:	NEXTIO.0402	Art Unit:	2112
Serial No.:	10/827117		
Filing Date:	4/19/04		
Title:	SWITCHING APPARATUS AND METHOD FOR PROVIDING SHARED I/O WITHIN A LOAD-STORE FABRIC		

PETITION TO MAKE SPECIAL UNDER 37 CFR 1.102(D)

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 CFR §1.102(d), applicant hereby petitions to make special the above identified patent application.

In compliance with the requirements of 37 CFR §1.102(d), and conforming to the recommendations of MPEP §708.02(VIII), applicant submits herewith the following:

a)   This petition, along with a check in the amount of $130 as set forth in 37 CFR 1.17(h).

b)   All claims in the above referenced patent application are directed to a single invention. If the Office determines that all the claims presented are not directed to a single invention, Applicant will make an election without traverse as a prerequisite to the grant of special status.

c)   Applicant submits that a pre-examination search was made, and reported on July 27, 2004 by Prior Art Searches, Inc.. A copy of the search report, along with a listing of the field of search, and the patents located is attached hereto. The search report references docket number Nextio.0301. Docket number Nextio.0402, contains a similar specification, differing in aspects of the disclosed invention which is claimed. A listing of the field of search class and subclass is located on page two of the search report from Prior Art Searches, Inc.

d)   Applicant submits herewith a copy of each of the references cited in the search report.

e)   DETAILED DISCUSSION OF THE REFERENCES

The search by Prior Art Searches, Inc. was directed towards a shared I/O switch fabric and controller for routing between different I/O devices and processing complexes. Additionally, the search was directed towards a shared I/O switch and controller which receives packets from a root complex or operating system domain and which places root complex or OSD identification information into the packets for routing purposes.

As mentioned in the search report, with respect to Ito et al. 5,581,709, an IO host adapter within a host computer gives a transaction a host number when the transaction is issued to a shared IO device (see Figure 3 of Ito). This teaching of requiring a host to identify itself with a unique number requires modification of host computers, which in today's PC market, is an unlikely scenario. Further, it does not allow for any IO initiated communication with a host. For example, if one of the IO cards 42 of Ito wishes to interrupt one of the host computers, it can't. It has no indication of what host numbers are associated with which host computers. In fact, all of the IO cards of Ito, and the extended IO apparatus 2, are completely ignorant of upstream hosts. There is no way for an IO card 42 to identify which of the host computers it wishes to communicate with. And, there is no teaching which allows the switch to detect or presume which host is intended to be communicated with, from the viewpoint of an extended IO apparatus. Presume that one of the IO cards of Ito is a network interface controller. And, that the network interface controller received a packet from a network to be transferred to one of

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the host computers. The IO card of Ito could not transfer the packet, because his IO card, and his extended IO apparatus, has no knowledge about the host computers north of the switch. Further, the IO switch 82 of Ito cannot pass any IO initiated communication back to the host. Thus, Ito only allows host initiated parallel communication to an IO card. Further, Ito only allows a single transaction to exist, at any point in time, between a host and an extended IO apparatus, causing all other communications from the same or other hosts to wait until completion.

With respect to Shaefer et al. 2004/0123014, he does not place root complex identification information into the packet. Shaefer deals with a cross-link devices within a PCI express architecture, and a root complex to bridge communications between a host system and switching elements. Shaefer does not teach anything related to shared I/O.
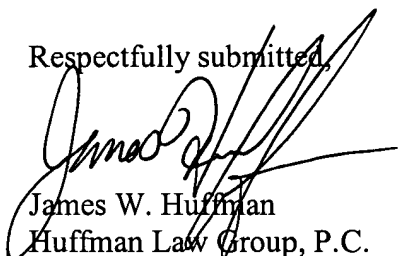
With respect to Chou (WO 94/19749), he does not discuss packets or identification of the processing complex in a request. In fact, Chou's invention is really directed at a switch for Nubus, PS/2, ISA, serial, and parallel devices to let 2 PC's (Mac and IBM) share the same peripherals.

In contrast, Applicant's invention as claimed, relates to a method and apparatus to allow multiple root complexes [or operating system domains, or PC's, or servers] to share one or more I/O devices, such as network interface controllers, disk drives, fiber channel controllers, etc. Applicant's invention allows communication from any host to an endpoint device, AND from any endpoint device to any host, without any change required in the host computer. In one embodiment, Applicant's invention is described utilizing a packet based serial communication protocol, particularly PCI-Express. In this environment, multiple transactions may exist at the same time between an endpoint device and one or more host computers. Nothing in the three references discussed above, or in any of the other patents disclosed in the search report teach these novel features.

For the foregoing reasons, Applicant believes that the instant application as embodied in the claims is novel over the cited art, and that a patent should issue therefrom. Applicant further believes that the above information satisfies the requirements specified in 37 CFR 1.102(d) for accelerated examination.

Applicant earnestly requests the Examiner to telephone him at the direct dial number printed below if the Examiner has any questions or suggestions concerning the application or allowance of any claims thereof.

Respectfully submitted,

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July 27, 2004

James W. Huffman, Esquire
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RE: **PETITION-TO-MAKE-SPECIAL SEARCH:**
SHARED I/O IN A LOAD/STORE FABRIC
YOUR REF: Nextio.0301
PAS NO: 04-19571

Dear Jim:

Pursuant your authorization and instruction letter of July 10, 2004 the above search has been conducted at the United States Patent and Trademark Office. The invention was described in your patent application. A report is presented below:

The search was directed towards a shared I/O switch fabric and controller for routing between different I/O devices and processing complexes. Additionally, the search was directed towards a shared I/O switch and controller which receives packets from a root complex (processing complex or core) or operating system domain (OSD) and which places root complex or OSD identification information into the packets for routing purposes.

The following U. S. patent and other documents have been developed during the investigation, and one copy of each is enclosed:

5,581,709	Ito et al.	2003/0079055	Chen
6,112,263	Futral	2004/0019714	Kelley et al.
6,247,077	Muller et al.	2004/0019726	Kelley et al.
6,662,254	Tal et al.	2004/0019729	Kelley et al.
6,760,793	Kelley et al.	2004/0123014	Schaefer et al.
2002/0078271	Berry	EP 0935200	NCR International, Inc.
2002/0172195	Pekkala et al.	WO 94/19749	Chou.

Ito et al. 5,581,709 discloses CPUs of a plurality of host computers accessing shared IO device. An IO host adaptor in the host computer gives a transaction a host number when the transaction is issued to a shared IO device. As shown in FIGs 8 & 11 and discussed throughout the specifications, each of the host computers has an IO host adaptor. That is, the identifier is – not- added in the switch fabric or switch controller in a centralized manner.

end page one / page two follows...

Schaefer et al. 2004/0123014 discloses a system of root complexes, switching fabric to route packetized communications between root complexes and peripheral devices (endpoints). FIG 2 shows a system of two hosts, each with a root complex and the associated switching components and peripherals. The switching elements may provide switching elements in accordance with PCI Express systems. However, Schaefer et al. does not discuss inserting root complex identification information into the packet.

Chou (WO 94/19749) discloses a switching interconnect module which connects two or more fully functional CPU-based microprocessor designs, such as MacIntosh-compatible and PC-compatible systems, to alternatively shared common system resources. The shared common system resources include a video display, user input means such as a keyboard or a mouse, input/output means such as a modem or printer, etc. The specification does not discuss packets or identification of the microprocessor involved in a request. Instead relying on switching by determining if requested device is available when requested and setting the route accordingly.

The prior art shows features such as a switch fabric and switching between host systems or root complexes, etc. and shared I/O devices or peripherals and also shows the use of packets in the transactions including use of identification information. However, the prior art does not show inserting the identifying information *after* the packet is received at the switch fabric.

The other documents were selected for your further review and disclose a switch fabric connecting root complexes and endpoints or show other individual features.

For your information the search included the following Patent Office classifications:

Class 370: MULTIPLEX COMMUNICATIONS
Subclass 351   PATHFINDING OR ROUTING
Subclass 389   . Switching a message which includes an address header
Subclass 392   .. Processing of address header for routing, per se
Subclass 422   .. Centralized switching
Subclass 912   PACKET COMMUNICATIONS
Subclass 913   . Wireless or radio

Class 710: ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING
              SYSTEMS: INPUT/OUTPUT
Subclass   1   INPUT/OUTPUT DATA PROCESSING
Subclass   2   . Input/Output addressing
Subclass 305   . Bus interface architecture
Subclass 306   .. Bus bridge
Subclass 313   ... Peripheral bus coupling (e.g., PCI, USB, ISA, and etc.)

The above subclasses were NOT searched additionally for foreign art and publication references. The foreign art and publication references housed in the examiners' search rooms are considered a supplemental search area. The PTO has not maintained these areas since approximately 1994. Therefore, they are considered optional.

     The search also included the Online Computer full text search (1970 to date) for various "key words" and character fields.
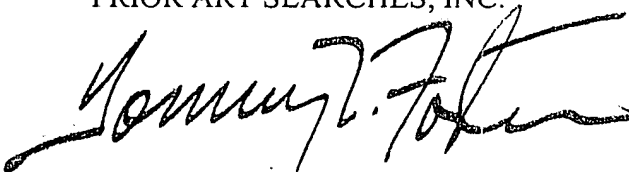
     In order to assure sufficiency of search the following examiner of the art unit indicated was consulted regarding the field of search: Joshua Kading (AU 2661).

     This search was conducted to meet the United States Patent Office (PTO) requirement for searches conduced in support of a Petition-to-Make Special and the individual conducting this search is formerly an examiner with the PTO for five years and who has a Master's Degree in Electrical and Computer Engineering.

     Kindly call if you have a question.

Very truly yours,

PRIOR ART SEARCHES, INC.

Tommy L. Foster, Senior Searcher

TLF/VAD:vad/ptv:0419571R
Enclosures